

Serial No. 10/675,841  
Unisys Corporation Docket No. RA-5635

Examiner Ryan A. Dare, Group Art Unit 2186  
Office Action Response – February 1, 2006

In the Claims:

**Claim 1 (Currently Amended)**

- 1           A control system, comprising:  
2           a storage device to store data signals and a mode designator, the mode  
3           designator to select a first or a second mode of operation;  
4           a circuit coupled to the storage device to receive as control signals  
5           predetermined ones of the data signals along with the mode designator, the  
6           control signals to control operation of the circuit when the circuit is operating in  
7           [a] the first mode; and  
8           Error Correction Code (ECC) logic coupled to the storage device to  
9           interpret the predetermined ones of the data signals as ECC check bits to detect  
10          errors in the data signals when the circuit is operating in [a] the second mode.

**Claim 2 (Original)**

- 1           The system of Claim 1, wherein the storage device is a memory having  
2           multiple addressable storage locations, each storing a different respective set of  
3           data signals.

**Claim 3 (Original)**

- 1           The system of Claim 2, wherein each of the addressable storage locations  
2           includes circuits to store a respective mode designator to control whether the  
3           circuit operates in the first or the second mode after the data signals stored at the  
4           addressable storage location are read from the memory.

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**Claim 4 (Original)**

- 1           The system of Claim 3, wherein the circuit includes branch logic to utilize  
2           the predetermined ones of the data signals stored at an addressable storage  
3           location to generate a next address for addressing the memory if the mode  
4           designator stored at the addressable storage location indicates the circuit will  
5           operate in the first mode.

**Claim 5 (Canceled)**

**Claim 6 (Original)**

- 1           The system of Claim 1, wherein the circuit includes logic to provide one or  
2           more functions of an instruction processor.

**Claim 7 (Original)**

- 1           The system of Claim 1, and further including a programmable storage  
2           device coupled to the circuit to select the predetermined ones of the data signals.

**Claim 8 (Original)**

- 1           The system of Claim 1, and further including at least one parity circuit  
2           coupled to the storage device to determine whether a parity error occurred on  
3           any of a predetermined set of the data signals.

**Claim 9 (Original)**

- 1           The system of Claim 8, wherein the at least one parity circuit includes a  
2           circuit to determine whether a parity error occurred on the predetermined set of  
3           the data signals when the circuit is operating in the second mode.

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**Claim 10 (Original)**

- 1           The system of Claim 1, wherein the ECC logic is coupled to ECC  
2 complement logic to correct errors in the data signals that are detected by the  
3 ECC logic when operating in the second mode.

**Claim 11 (Original)**

- 1           The system of Claim 10, and further including logic coupled to the ECC  
2 complement logic to provide the data signals to the circuit for use as control  
3 signals after any errors detected by the ECC logic have been corrected.

**Claim 12 (Currently Amended)**

- 1           A method of controlling a digital system, comprising:  
2           a.) reading first data signals along with a mode indicator from a storage  
3 device;  
4           b.) interpreting the first data signals as control signals to control one or  
5 more functions of the digital system if operating in a first mode of operation as  
6 determined by a state of the mode indicator; and  
7           c.) interpreting the first data signals as Error Correction Code (ECC)  
8 signals if operating in a second mode of operation as determined by the state of  
9 the mode indicator.

**Claim 13 (Original)**

- 1           The method of Claim 12, and further including:  
2           reading second data signals from the storage device; and  
3           using the ECC signals to detect errors in the second data signals if  
4 operating in the second mode of operation.

**Claim 14 (Original)**

- 1           The method of Claim 13, wherein the storage device is a memory, and  
2 wherein the first and second data signals are stored at a same addressable  
3 location within the memory.

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**Claim 15 (Original)**

- 1           The method of Claim 14, wherein multiple memory addresses each stores  
2 different respective first and second data signals.

**Claim 16 (Original)**

- 1           The method of Claim 15, and further including using the first data signals  
2 to generate a next address for addressing the memory when operating in the first  
3 mode of operation.

**Claim 17 (Currently Amended)**

- 1           The method of Claim 15, and further including:  
2           reading one of the multiple memory addresses; and  
3           interpreting at least one of the second data signals as [a] the mode  
4 indicator to indicate whether operation is occurring in the first or the second  
5 mode of operation.

**Claim 18 (Currently Amended)**

- 1           The method of Claim 17, and including repeating the steps of Claim 17 for  
2 each of multiple memory addresses.

**Claim 19 (Original)**

- 1           The method of Claim 13, and further including, correcting an error if the  
2 error is detected in predetermined ones of the second data signals.

**Claim 20 (Original)**

- 1           The method of Claim 19, and further including programmably selecting the  
2 predetermined ones of the second data signals.

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**Claim 21 (Original)**

- 1           The method of Claim 12, and further including programmably selecting the  
2 first data signals.

**Claim 22 (Original)**

- 1           The method of Claim 13, and further including interpreting one or more of  
2 the second data signals as control signals to control an arithmetic logic unit of an  
3 instruction processor.

**Claim 23 (Original)**

- 1           The method of Claim 13, an further including using parity bits to detect a  
2 parity error occurring within the first or the second data signals.

**Claim 24 (Original)**

- 1           The method of Claim 23, and further including:  
2           reporting any error detected using the ECC signals; and  
3           reporting any error detected using the parity bits.

**Claim 25 (Original)**

- 1           The method of Claim 24, and further including:  
2           servicing any error detected by the ECC signals at a time that is optimal  
3 for the digital system; and  
4           servicing any error detected using the parity bits substantially immediately.

**Claim 26 (Currently Amended)**

- 1           A control system having a first and second mode of operation, comprising:  
2           storage means for storing data signals and a mode designator, a state of  
3 the mode designator selecting between operation in the first mode or the second  
4 mode;

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- 5 control means for receiving the data signals with the mode designator, and  
6 for utilizing first ones of the data signals to affect operations of the control system  
7 when operating in the first mode; and  
8 error means for interpreting the first ones of the data signals as check bits  
9 for detecting errors occurring in second ones of the data signals when the  
10 control system is operating in the second mode.

**Claim 27 (Currently Amended)**

- 1 The system of Claim 26, wherein the storage means includes means for  
2 storing [a] the mode designator to control whether the control system is operating  
3 in the first or the second mode.

**Claim 28 (Original)**

- 1 The system of Claim 26, wherein the control means includes branch  
2 means for utilizing the first ones of the data signals to generate an address for  
3 the storage means.

**Claim 29 (Original)**

- 1 The system of Claim 26, wherein the storage means is a memory  
2 including predetermined addressable locations, each storing a different  
3 respective set of the first and second ones of the data signals.

**Claim 30 (Original)**

- 1 The system of Claim 29, wherein each of the predetermined addressable  
2 locations within the memory includes means for storing a mode designator for  
3 controlling whether the control system operates in the first or the second mode  
4 when the first and the second ones of the data signals stored at the addressable  
5 location are read from the memory.

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**Claim 31 (Original)**

- 1       The system of Claim 30, wherein the error means includes means for  
2       correcting an error detected on predetermined ones of the second ones of the  
3       data signals when the control system is operating in the second mode.

**Claim 32 (Original)**

- 1       The system of Claim 31, and further including means for providing  
2       corrected ones of the second ones of the data signals to the control means for  
3       use in affecting the operations of the control system.

**Claim 33 (Original)**

- 1       The system of Claim 31, and further including parity detection means for  
2       detecting parity errors within the first or the second ones of the data signals.

**Claim 34 (Original)**

- 1       The system of Claim 33, wherein the parity detection means includes  
2       means for detecting uncorrected parity errors remaining within the second ones  
3       of the data signals.

**Claim 35 (Original)**

- 1       The system of Claim 33, and further including maintenance means for  
2       performing error recovery actions within a first time period for errors detected by  
3       the parity detection means and, for errors detected by the error means,  
4       performing error recovery actions any time the control system is appropriately  
5       configured.

**Claim 36 (Original)**

- 1       The system of Claim 26, and further including means for programmably  
2       selecting the first ones of the data signals.

**Claim 37 (Original)**

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The system of Claim 31, and further including means for programmably selecting the predetermined ones of the second ones of the data signals.